44-GHz High-Efficiency InP-HEMT MMIC Power Amplifier

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***Abstract*—A high-efficiency power amplifier was developed using 0.15-μm gatelength, InP-based (GaInAs/AlInAs/InP), HEMT MMIC technology. The amplifier demonstrated state-of-the-art performance. The output power at 1-dB compression point was 28 dBm at 44.5 GHz. The corresponding power-added efficiency was 31% and gain was 7 dB. The total chip area was 2.5 mm^2.**

I. Introduction

High electron mobility transistor (HEMT) monolithic millimeter-wave integrated circuit (MMIC) technology is developing rapidly for power applications. High-efficiency MMIC power amplifier enables man-portable communication terminals and phased arrays. Aust *et al.* [1] developed a 2-stage power amplifier with 0.15-μm GaAs-based (InGaAs/AlGaAs/GaAs) HEMT MMIC technology. The amplifier demonstrated 30-dBm output power, 20% power-added efficiency, and 9-dB gain at 35 GHz. Huang *et al.* [2] developed a 2-stage power amplifier with 0.2-μm GaAs-based HEMT MMIC technology. That amplifier exhibited 27-dBm output power, 15% power added efficiency, and 7-dB gain at 40 GHz. In this letter, we report the development of a single-stage power amplifier using 0.15-μm InP-based HEMT MMIC technology. InP-based HEMT offers higher power-added efficiency, gain, and lower channel temperature than GaAs-based HEMT.

II. Design

A large signal model of the power HEMT was developed to design the amplifier on LIBRA circuit simulator [3]. The device had six gate fingers and the length of each finger was 75 μm. The measured IV curve was fitted to the Curtice's nonlinear FET model, and the measured scattering parameter was fitted to the conventional FET equivalent circuit, whose parasitic elements were determined from measurement taken from the cold bias condition.

The design was a single-stage amplifier suitable for solid-state power amplifier development. Fig. 1 shows the design. The input and output matching networks provided power combining and impedance transformation to the power HEMT's.

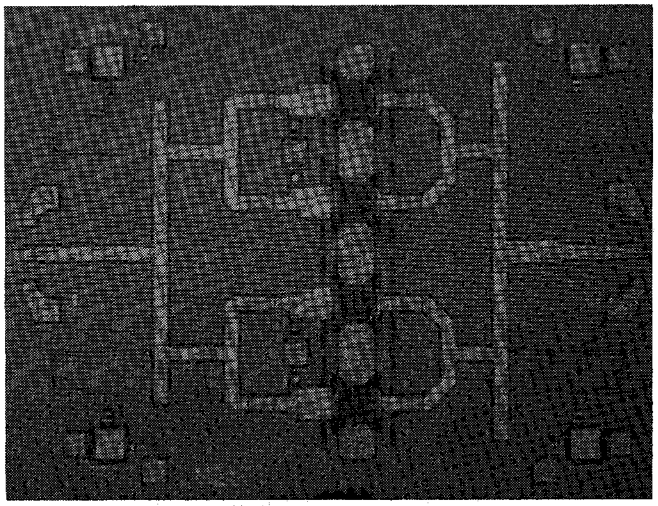

Fig. 1. Power MMIC amplifier.

The input network employed metal-insulator-metal (MIM) capacitors to minimize its physical size. The stability networks utilized a combination of lump-element resistor, a quarter-wavelength transmission line, and a MIM capacitor to suppress even-mode oscillation, and lumped-element resistors to suppress odd-mode oscillation [4]. The physical dimensions of the amplifier chip were 1.4 by 1.8 mm. The substrate thickness was 50 μm.

III. Fabrication

The power amplifier was fabricated with our standard 0.15-μm T-gate InP-based HEMT MMIC process [3]. Fig. 2 shows the device cross-section of the power HEMT, which typically achieves a transconductance peak of 600 mS/mm and a maximum drain current of 600 mA/mm. The typical current cutoff frequency is 120 GHz. The gate-drain breakdown voltage is 9 V, measured at 1 mA/mm of current density. The power HEMT is capable of greater than 500 mW/mm output power density and 30% power-added efficiency at Q-band frequencies. Other MMIC components available are microstrip transmission lines, airbridges, MIM capacitor, channel resistor, and via hole.

IV. Result

The small signal performance of the power amplifier was measured on wafer using Cascade Microtech probes and the Wiltron network analyzer. The measurement system was

Manuscript received April 6, 1994. This work was sponsored by MILSTAR System Program Office (ESD/MS), Electronic Systems Division, Hanscom Air Force Base, Bedford, MA 01731 USA.

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IEEE Log Number 9403582.

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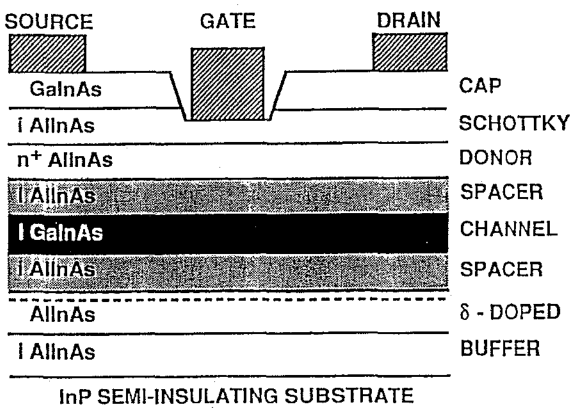

Fig. 2. InP-Based HEMT cross-section.

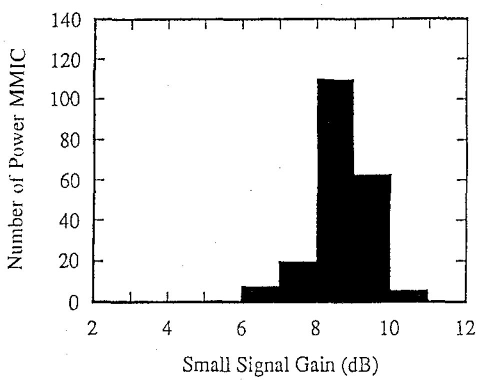

Fig. 3. Measured small signal gain histogram.

calibrated with the through-reflect-match technique. Fig. 3 shows a histogram of the measured small-signal gain from a 2-inch wafer. The average small-signal gain was 8.7 dB and the standard deviation was 0.7 dB at 44.5 GHz. The RF functional yield (for amplifier gain >6 dB) was 47%. The power performance of the amplifier was measured on test fixture using E-plane probe transitions. The measured insertion loss of the overall test fixture was 1.4 dB at 44.5 GHz, which was used to de-embed the performance of the power MMIC. The amplifier was biased at class AB condition for simultaneous high efficiency, power, and gain operation. The drain current was 400 mA and the drain voltage was 3.8 V. Fig. 4 shows the measured output power and power-added efficiency at 44.5 GHz. The output power at 1-dB compression point was 28 dBm at 44.5 GHz. The corresponding power-added efficiency was 31% and associated gain was 7 dB.

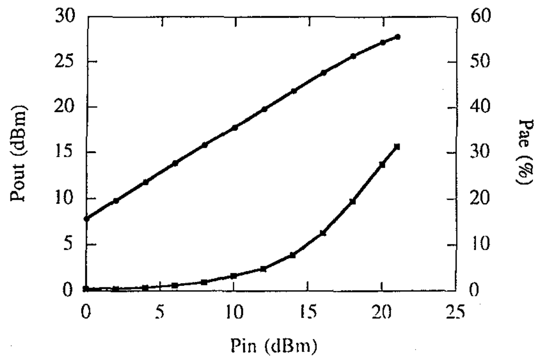

Fig. 4. Measured output power and efficiency.

V. Conclusion

A high-efficiency power amplifier was developed using 0.15-μm InP-based HEMT MMIC technology. The amplifier demonstrated state-of-the-art performance (28-dBm output power, 31% power-added efficiency, and 7-dB gain at 44.5 GHz). The technology is developing very rapidly. Recent advance in improving the breakdown voltage of InP-based HEMT to 20 V suggests even higher performances are possible [5].

Acknowledgment

The authors would like to thank R. Lohr for layout support, S. Rosenbaum for device measurement assistance, D. Pierson for MMIC post process, H. Nghiem and M. Tran for MMIC evaluation, and J. Chen and R. Ying for technical suggestions. We would also like to thank the MILSTAR System Program Office, Hanscom, for their foresight and encouragement in sponsoring the amplifier development.

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